4 Ω R_{ON}, 4-/8-Channel ±15 V/+12 V/±5 V *i*CMOS™ Multiplexers

ADG1408/ADG1409

FEATURES

4.7 Ω maximum on resistance @ 25°C
0.5 Ω on resistance flatness
33 V supply maximum ratings
Fully specified at ±15 V/+12 V/±5 V
3 V logic-compatible inputs
Rail-to-rail operation
Break-before-make switching action
16-lead TSSOP and 4 mm × 4 mm LFCSP_VQ packages

APPLICATIONS

Relay replacement
Audio and video routing
Automatic test equipment
Data acquisition systems
Temperature measurement systems
Avionics
Battery-powered systems
Communication systems
Medical equipment

FUNCTIONAL BLOCK DIAGRAM

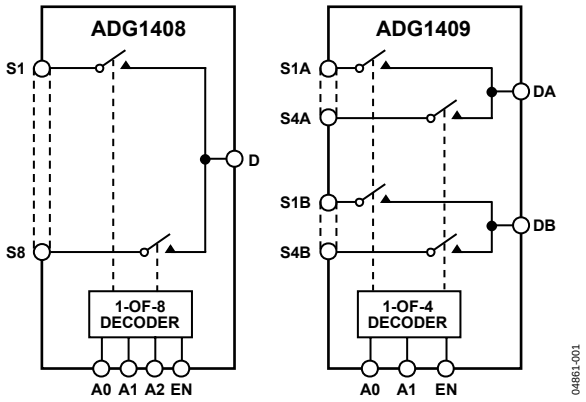

Figure 1.

GENERAL DESCRIPTION

The ADG1408/ADG1409 are monolithic *i*CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1408 switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG1409 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow on resistance and on resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 4 Ω on resistance.
2. 0.5 Ω on resistance flatness.
3. 3 V logic compatible digital input, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. 16-lead TSSOP and 4 mm × 4 mm LFCSP_VQ package.

Table 1. Related Devices

Part No.	Description
ADG1208/ADG1209	Low capacitance, low charge injection, and low leakage 4-/8-channel ±15 V multiplexers

Rev. 0

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REVISION HISTORY

8/06—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	4			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 26
	4.7	5.7	6.7	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	0.2			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.78	0.85	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.72	0.77	0.92	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (OFF)	±0.04			nA typ	V_S = ±10 V, V_S = ∓10 V; see Figure 27
	±0.2	±0.6	±5	nA max	
Drain Off Leakage, I_D (OFF)	±0.04			nA typ	V_S = ±10 V, V_S = ∓10 V; see Figure 27
	±0.45	±2	±30	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 28
	±1.5	±3	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	140			ns typ	R_L = 100 Ω, C_L = 35 pF
	170	210	240	ns max	V_S = 10 V, see Figure 29
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 100 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 30
t_{ON} (EN)	100			ns typ	R_L = 100 Ω, C_L = 35 pF
	120	150	165	ns max	V_S = 10 V; see Figure 31
t_{OFF} (EN)	100			ns typ	R_L = 100 Ω, C_L = 35 pF
	120	150	170	ns max	V_S = 10 V; see Figure 31
Charge Injection	−50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Total Harmonic Distortion, THD + N	0.025			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 36
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35
ADG1408	60			MHz typ	
ADG1409	115			MHz typ	
Insertion Loss	0.24			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
C_S (OFF)	14			pF typ	f = 1 MHz
C_D (OFF)					
ADG1408	80			pF typ	f = 1 MHz
ADG1409	40			pF typ	f = 1 MHz
C_D, C_S (ON)					
ADG1408	135			pF typ	f = 1 MHz
ADG1409	90			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
I_{DD}	220			µA typ	Digital inputs = 5 V
			325	µA max	
I_{SS}	0.002			µA typ	Digital inputs = 0 V, 5 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	

[1] Temperature range: Y version: −40 °C to +125 °C.
[2] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 26
	8	9.5	11.2	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	0.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.82	0.85	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	2.5	2.5	2.8	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage, I_S (OFF)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.2	±0.6	±5	nA max	
Drain Off Leakage, I_D (OFF)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.45	±1	±37	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.06			nA typ	V_S = V_D = 1 V or 10 V; see Figure 28
	±0.44	±1.3	±32	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	200			ns typ	R_L = 100 Ω, C_L = 35 pF
	260	330	380	ns max	V_S = 8 V; see Figure 29
Break-Before-Make Time Delay, t_D	90			ns typ	R_L = 100 Ω, C_L = 35 pF
			40	ns min	V_{S1} = V_{S2} = 8 V; see Figure 30
t_{ON} (EN)	160			ns typ	R_L = 100 Ω, C_L = 35 pF
	210	250	285	ns max	V_S = 8 V; see Figure 31
t_{OFF} (EN)	115			ns typ	R_L = 100 Ω, C_L = 35 pF
	145	180	200	ns max	V_S = 8 V; see Figure 31
Charge Injection	−12			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
OFF Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35
ADG1408	36			MHz typ	
ADG1409	72			MHz typ	
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
C_S (OFF)	25			pF typ	f = 1 MHz
C_D (OFF)					
ADG1408	165			pF typ	f = 1 MHz
ADG1409	80			pF typ	f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
C_D, C_S (ON)					
ADG1408	200			pF typ	f = 1 MHz
ADG1409	120			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
I_{DD}	220			µA typ	Digital inputs = 5 V
			335	µA max	
V_{DD}			5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	7			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 26
	9	10.5	12	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between Channels (ΔR_{ON})	0.3			Ω typ	V_S = ±4.5V, I_S = −10 mA
	0.78	0.91	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5			Ω typ	V_S = ±4.5 V; I_S = −10 mA
	2.5	2.5	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (OFF)	±0.02			nA typ	V_S = ±4.5 V, V_S = ∓4.5 V; see Figure 27
	±0.2	±0.6	±5	nA max	
Drain Off Leakage, I_D (OFF)	±0.02			nA typ	V_S = ±4.5 V, V_S = ∓4.5 V; see Figure 27
	±0.45	±0.8	±20	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.04			nA typ	V_S = V_D = ±4.5 V; see Figure 28
	±0.3	±1.1	±22	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current	±0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	330			ns typ	R_L = 100 Ω, C_L = 35 pF
	440	530	550	ns max	V_S = 5 V; see Figure 29
Break-Before-Make Time Delay, t_D	100			ns typ	R_L = 100 Ω, C_L = 35 pF
			50	ns min	V_{S1} = V_{S2} = 5 V; see Figure 30
t_{ON} (EN)	245			ns typ	R_L = 100 Ω, C_L = 35 pF
	330	400	440	ns max	V_S = 5 V; see Figure 31
t_{OFF} (EN)	215			ns typ	R_L = 100 Ω, C_L = 35 pF
	285	335	370	ns max	V_S = 5 V; see Figure 31
Charge Injection	−10			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 34
Total Harmonic Distortion, THD + N	0.06			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 36
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF; see Figure 35
ADG1408	40			MHz typ	
ADG1409	80			MHz typ	
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
C_S (OFF)	20			pF typ	f = 1 MHz
C_D (OFF)					
ADG1408	130			pF typ	f = 1 MHz
ADG1409	65			pF typ	f = 1 MHz
C_D, C_S (ON)					
ADG1408	180			pF typ	f = 1 MHz
ADG1409	120			pF typ	f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V, 5 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	

[1] Temperature range for Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature (Pb-Free)	260(+0/−5)°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16 Lead TSSOP	150.4	50	°C/W
16-Lead LFCSP_VQ	30.4		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

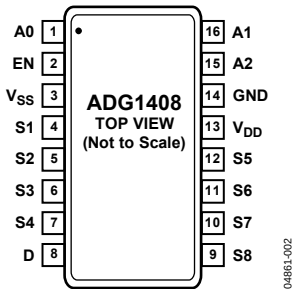


Figure 2. ADG1408 Pin Configuration (TSSOP)

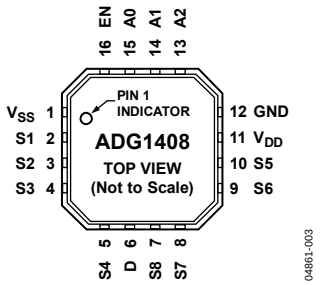


Figure 3. ADG1408 Pin Configuration (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 7. ADG1408 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	2	S1	Source Terminal 1. Can be an input or an output.
5	3	S2	Source Terminal 2. Can be an input or an output.
6	4	S3	Source Terminal 3. Can be an input or an output.
7	5	S4	Source Terminal 4. Can be an input or an output.
8	6	D	Drain Terminal. Can be an input or an output.
9	7	S8	Source Terminal 8. Can be an input or an output.
10	8	S7	Source Terminal 7. Can be an input or an output.
11	9	S6	Source Terminal 6. Can be an input or an output.
12	10	S5	Source Terminal 5. Can be an input or an output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	GND	Ground (0 V) Reference.
15	13	A2	Logic Control Input.
16	14	A1	Logic Control Input.

Table 8. ADG1408 Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

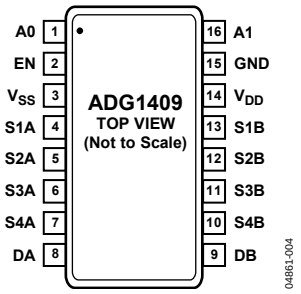


Figure 4. ADG1409 Pin Configuration (TSSOP)

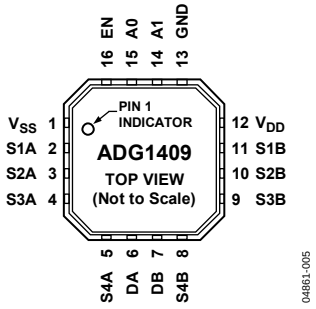


Figure 5. ADG1409 Pin Configuration (LFCSP_VQ), Exposed Pad Tied to Substrate, V_{SS}

Table 9. ADG1409 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	2	S1A	Source Terminal 1A. Can be an input or an output.
5	3	S2A	Source Terminal 2A. Can be an input or an output.
6	4	S3A	Source Terminal 3A. Can be an input or an output.
7	5	S4A	Source Terminal 4A. Can be an input or an output.
8	6	DA	Drain Terminal A. Can be an input or an output.
9	7	DB	Drain Terminal B. Can be an input or an output.
10	8	S4B	Source Terminal 4B. Can be an input or an output.
11	9	S3B	Source Terminal 3B. Can be an input or an output.
12	10	S2B	Source Terminal 2B. Can be an input or an output.
13	11	S1B	Source Terminal 1B. Can be an input or an output.
14	12	V_{DD}	Most Positive Power Supply Potential.
15	13	GND	Ground (0 V) Reference.
16	14	A1	Logic Control Input.

Table 10. ADG1409 Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

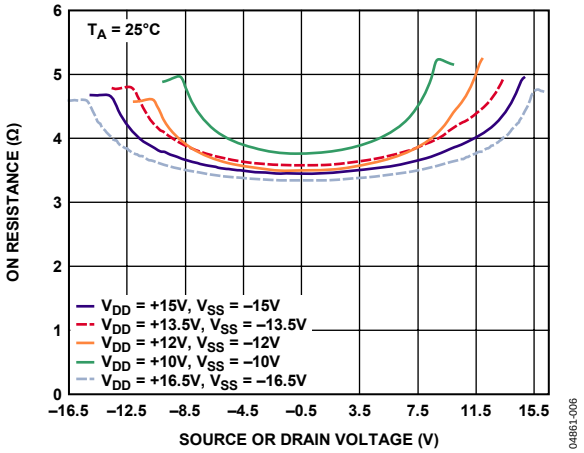


Figure 6. On Resistance as a Function of V_D (V_S), Dual Supply

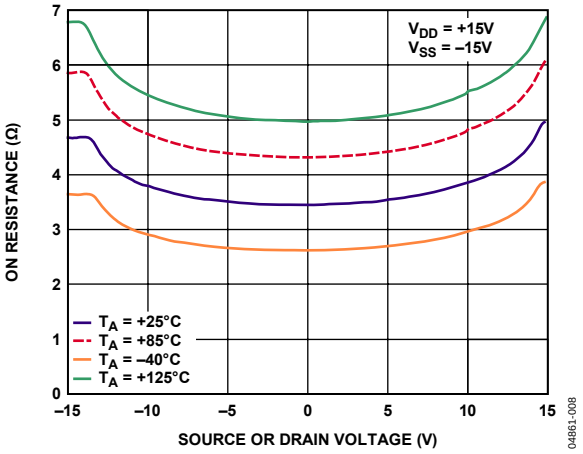


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, 15 V Dual Supply

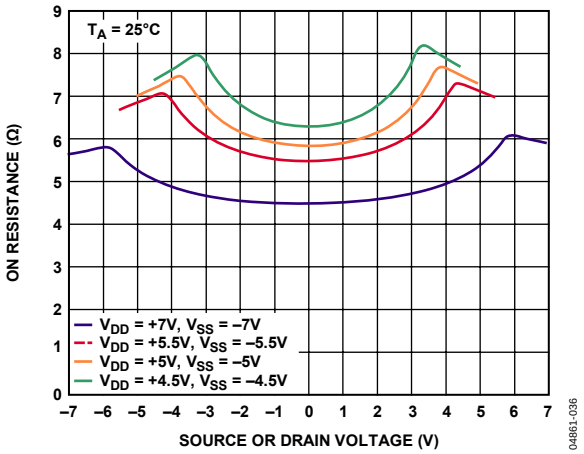


Figure 7. On Resistance as a Function of V_D (Vs), Dual Supply

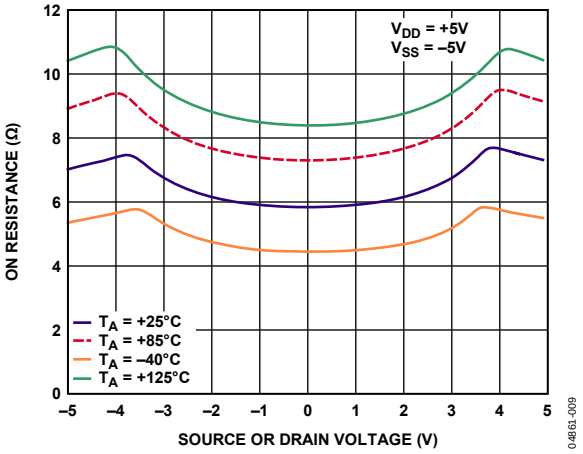


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Dual Supply

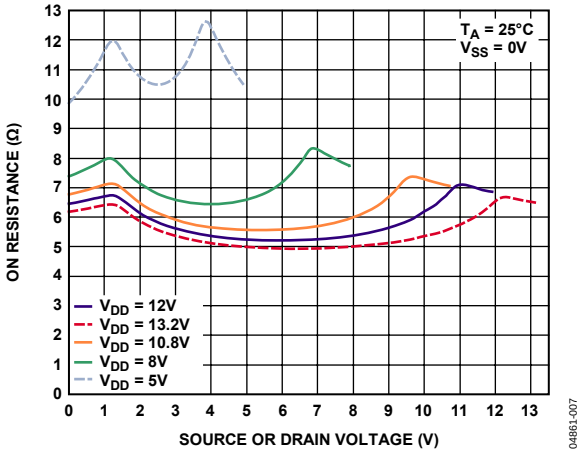


Figure 8. On Resistance as a Function of V_D (V_S), Single Supply

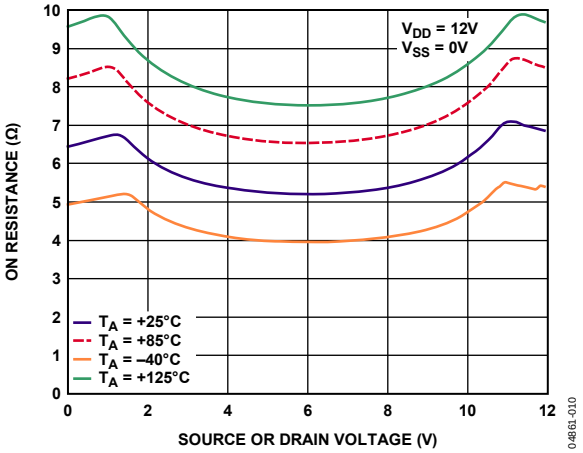


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

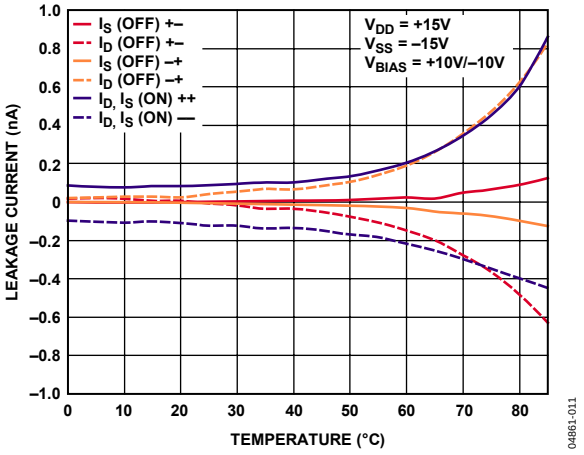


Figure 12. Leakage Currents as a Function of Temperature, 15 V Dual Supply

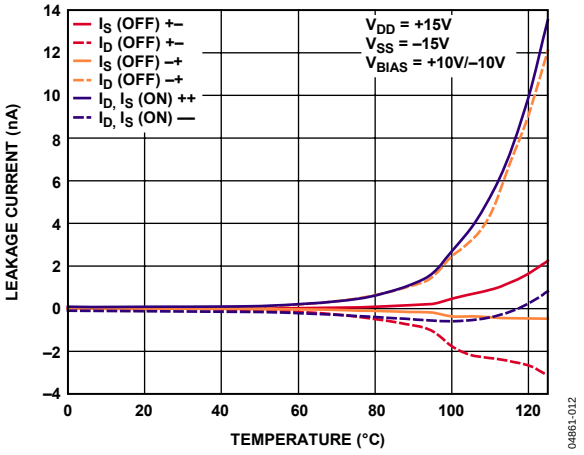


Figure 13. Leakage Currents as a Function of Temperature, 15 V Dual Supply

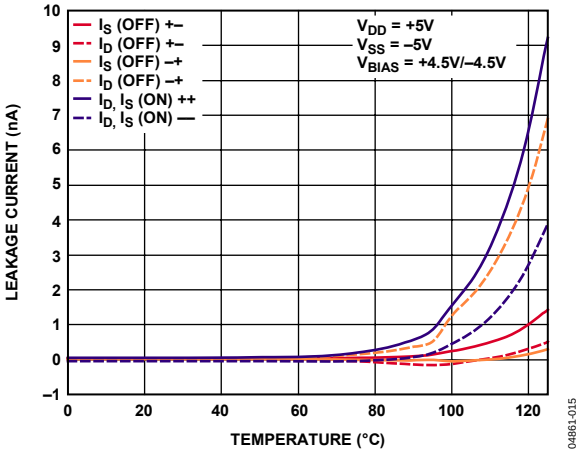


Figure 14. Leakage Currents as a Function of Temperature, 5 V Dual Supply

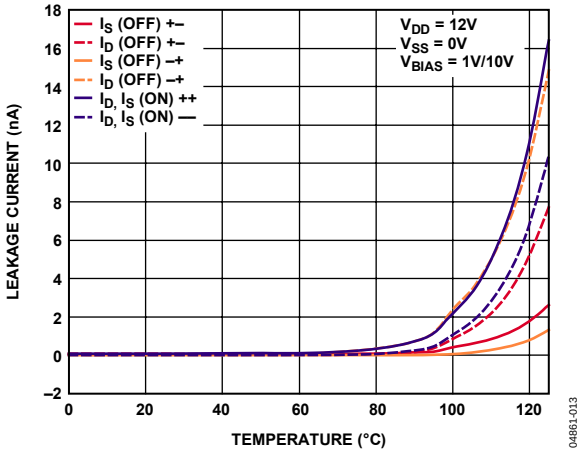


Figure 15. Leakage Currents as a Function of Temperature, 12 V Single Supply

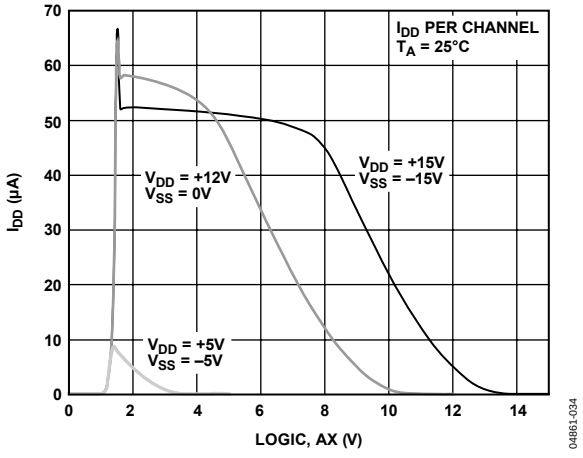


Figure 16. I_{DD} vs. Logic Level

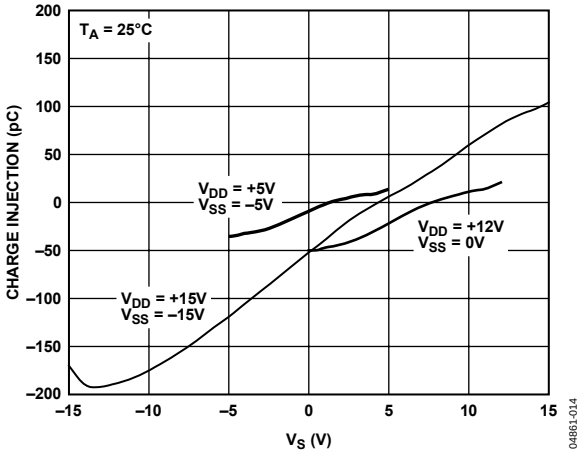


Figure 17. Charge Injection vs. Source Voltage

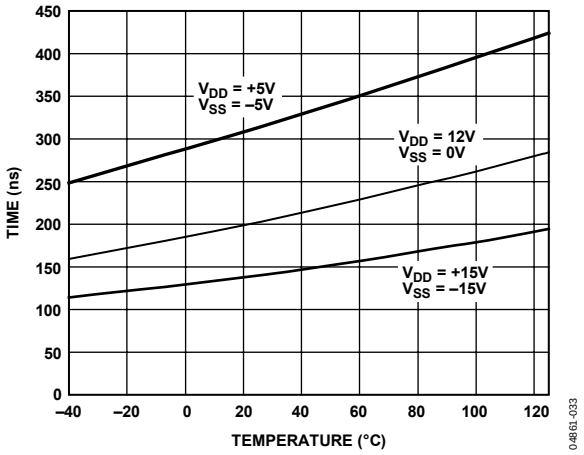


Figure 18. Transition Time vs. Temperature

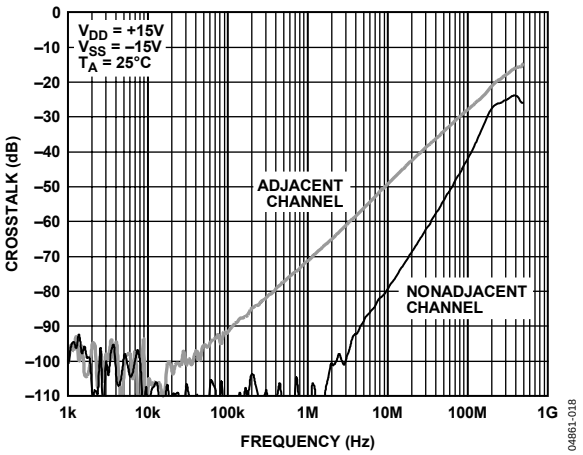


Figure 21. ADG1409 Crosstalk vs. Frequency

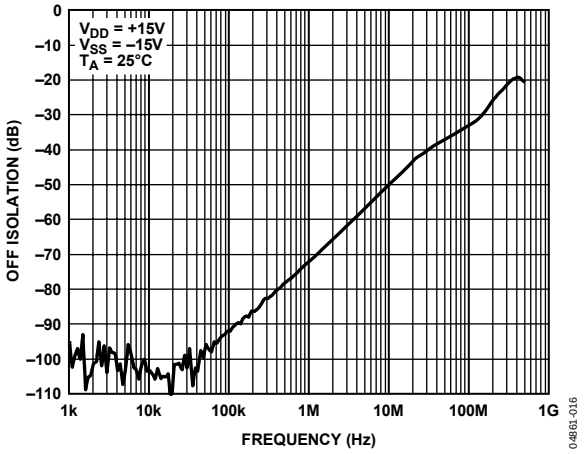


Figure 19. Off Isolation vs. Frequency

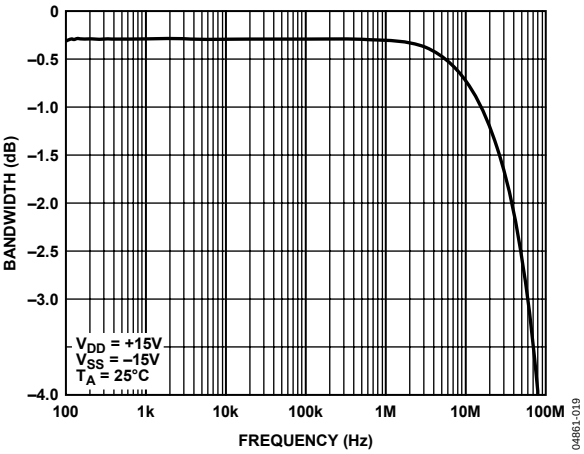


Figure 22. ADG1408 On Response vs. Frequency

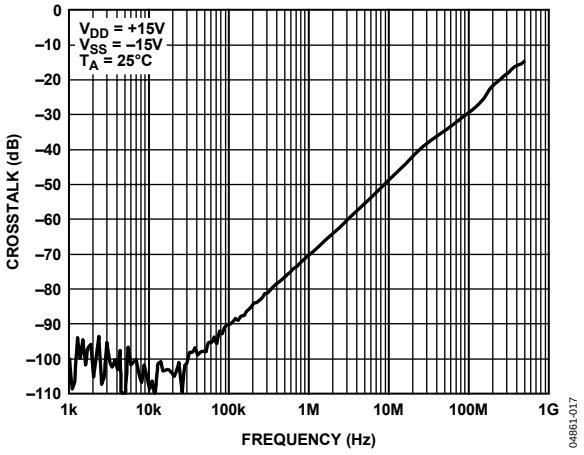


Figure 20. ADG1408 Crosstalk vs. Frequency

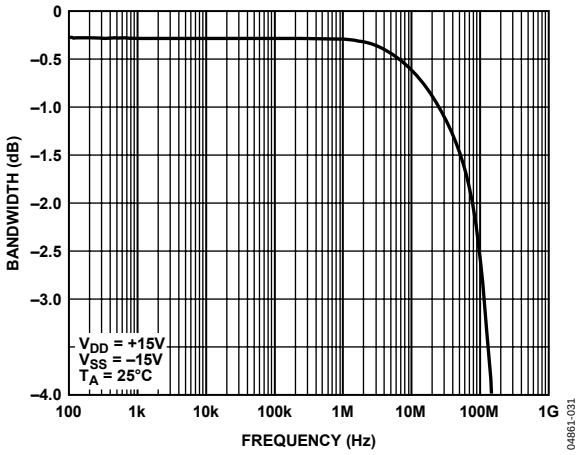


Figure 23. ADG1409 On Response vs. Frequency

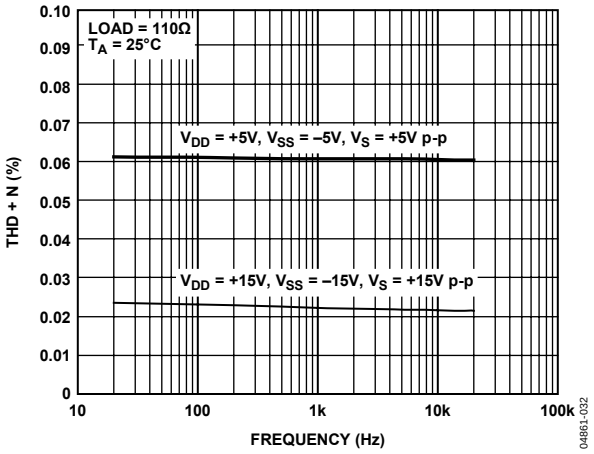


Figure 24. THD + N vs. Frequency

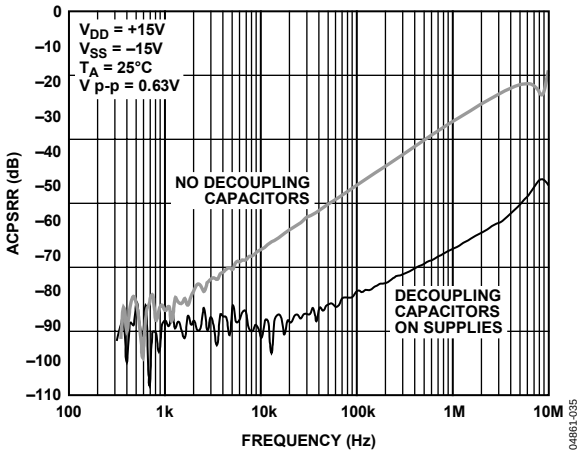


Figure 25. ACPSRR vs. Frequency

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (OFF)
Source leakage current when the switch is off.

I_D (OFF)
Drain leakage current when the switch is off.

I_D, I_S (ON)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

C_S (OFF)
Channel input capacitance for off condition.

C_D (OFF)
Channel output capacitance for off condition.

C_D, C_S (ON)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

Total Harmonic Distortion (THD + N)
Ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

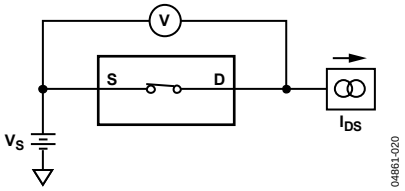


Figure 26. On Resistance

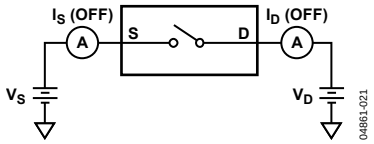


Figure 27. Off Leakage

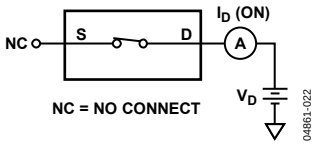


Figure 28. On Leakage

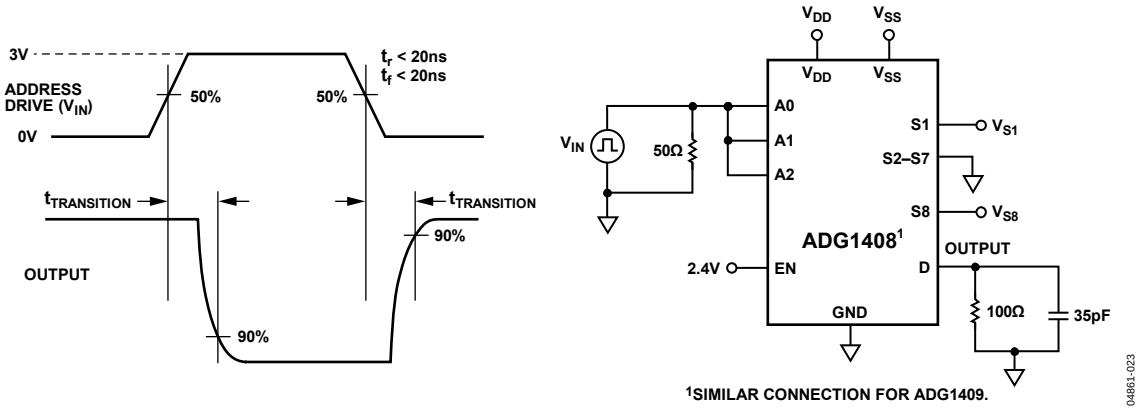


Figure 29. Address to Output Switching Times, $t_{TRANSITION}$

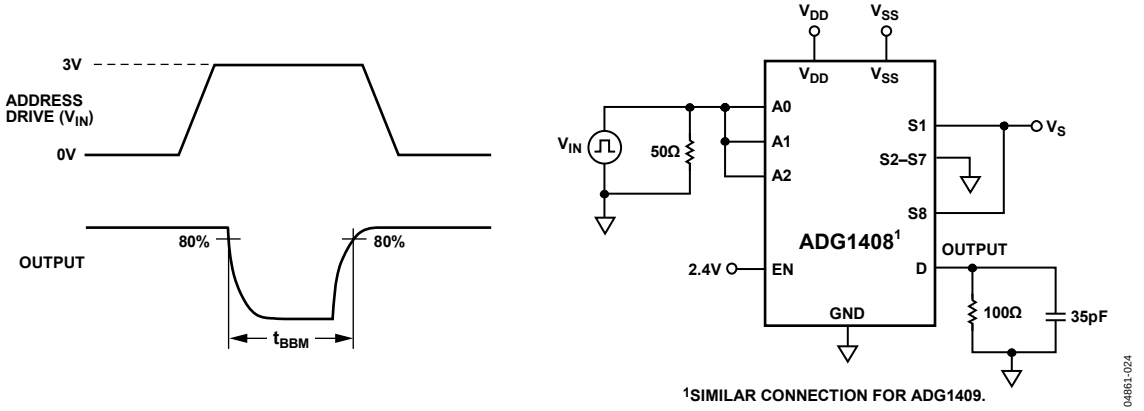


Figure 30. Break-Before-Make Delay, t_{BBM}

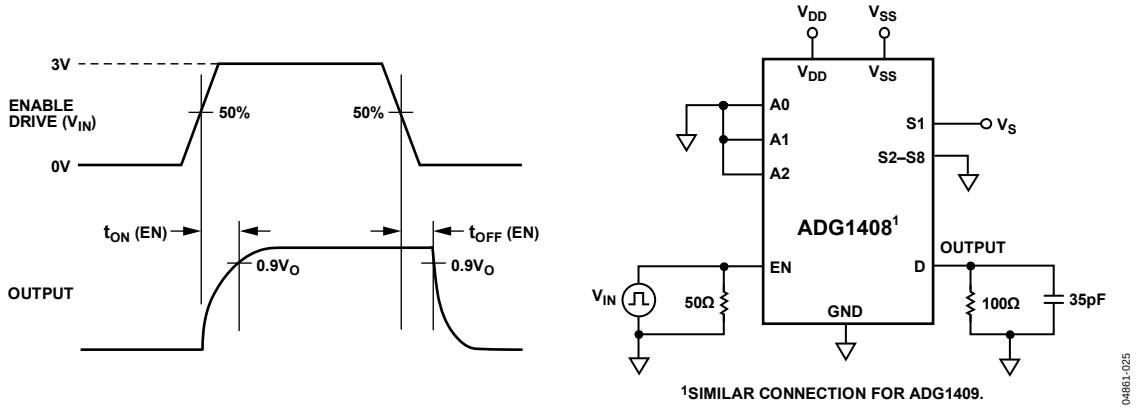


Figure 31. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

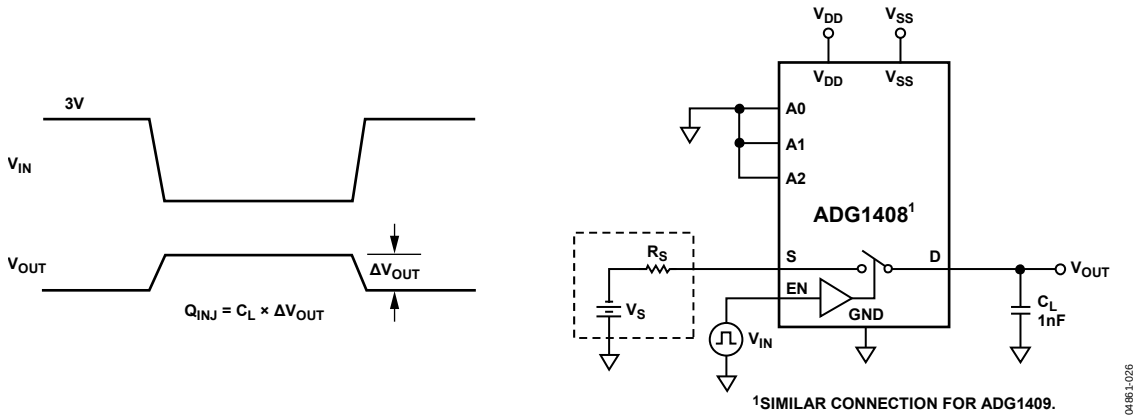


Figure 32. Charge Injection

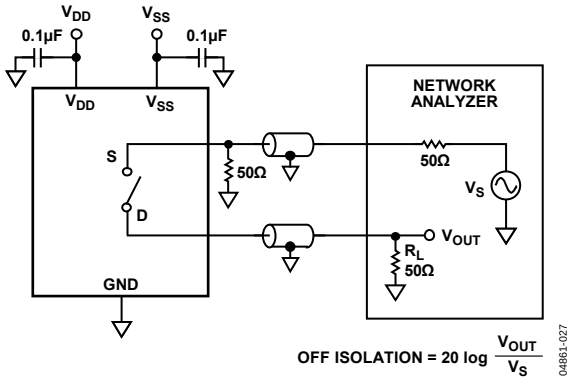


Figure 33. Off Isolation

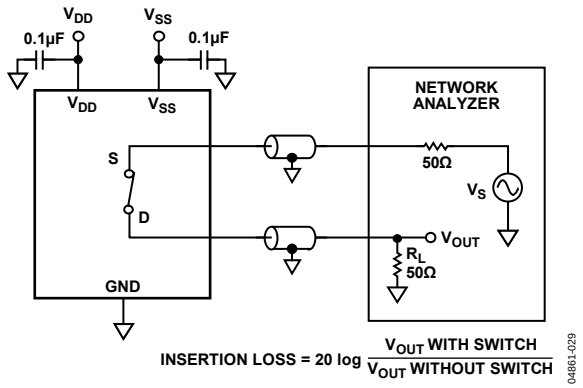


Figure 35. Insertion Loss

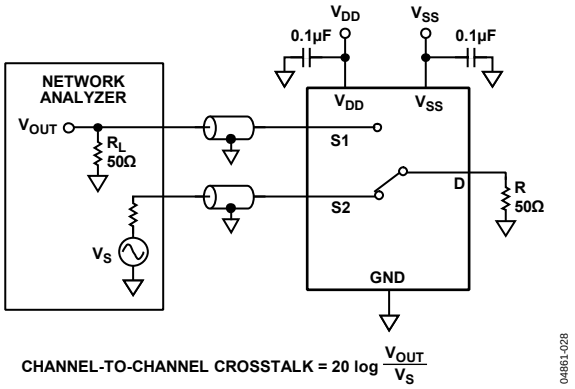


Figure 34. Channel-to-Channel Crosstalk

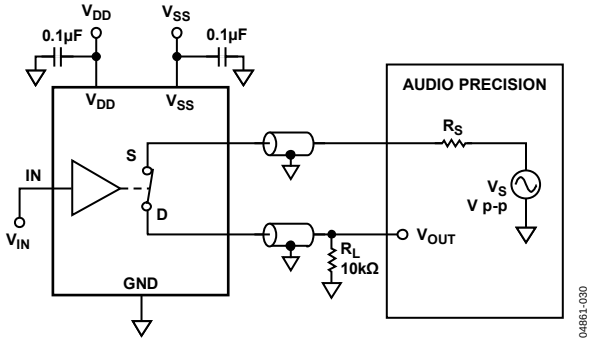
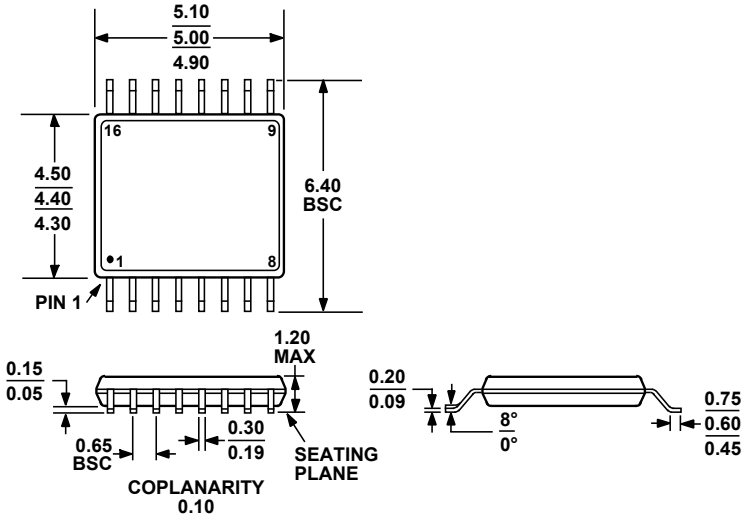


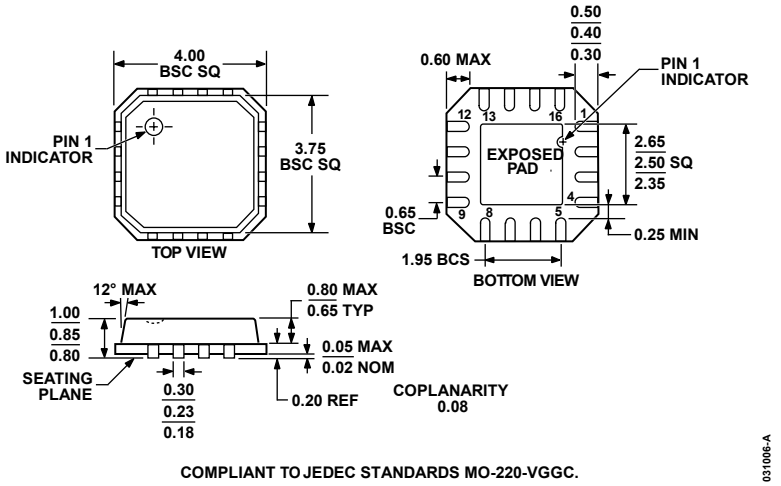
Figure 36. THD + Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm, Very Thin Quad (CP-16-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1408YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408YRUZ-REEL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-13
ADG1409YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409YRUZ-REEL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-13

[1] Z = Pb-free part.

NOTES

D04861-0-8/06(0)